WHAT IS CLAIMED IS:

1. A method of simultaneously testing analog-to-digital converters (ADC) on a plurality of chips on a wafer comprising:

connecting a first group of the plurality of chips to a first power line and connecting a second group of plurality of chips to a second power line;

applying a power signal to said first power line;

simultaneously running ADC test procedures on each of said first group of chips connected to said first of the power lines during said applying; and

reporting test results for each of the chips in the first group.

2. The method of claim 1, further comprising repeating said applying said simultaneously running, and said reporting, for said second group and said second power line.

3. The method of claim 1, further comprising the test procedures comprising:

setting a light condition;

obtaining a first ADC output after a first integration time;

obtaining a second ADC output after a second integration time;

comparing the first ADC output to the second ADC output, wherein the test results are failed if the second ADC output is less than the first ADC output.

4. The method of claim 1, further comprising forming a test engine that embeds the test procedures.

5. The method of claim 1, wherein said connecting comprises including first and second power lines on the wafer.

6. The method of claim 1, wherein said connecting comprises connecting the plurality of chips said power lines by overlaying the wafer with a test template, wherein the test template includes the one or more power lines.

7. The method of claim 6, further comprising forming a test engine on said template that embeds the test procedures test engine.

8. A wafer comprising:

a plurality of chips, wherein each of the plurality of chips includes an analog-to-digital converter;

one or more power lines connecting at least a portion of the plurality of chips, wherein the one or more power lines interconnect the portion of the plurality of chips to simultaneously run ADC test procedures on each chip in the portion of the plurality of chips.

9. The wafer of Claim 8, further comprising a test engine connected to the plurality of chips.

10. The wafer of Claim 9, wherein the test engine includes said ADC test procedures.

11. A wafer test system comprising:

a wafer including a plurality of chips, wherein each of the plurality of chips includes an analog-to-digital converter (ADC);

a template including one or more power lines and a plurality of vias which correspond to the plurality of chips on the wafer, wherein the template is adapted to interface with the wafer so the one or more power lines interconnect at least a portion of the plurality of chips to simultaneously run ADC test procedures on each chip in the portion of the plurality of chips.

12. The wafer of Claim 11, further comprising a test engine on the template.

13. The wafer of Claim 12, wherein the test engine includes the test procedures.

14. An assembly, comprising:

a wafer including a plurality of separable image elements thereon, arranged in groups, each group having a plurality of said image elements therein;

a plurality of power lines, one of said power lines arranged for each group, and arranged to provide a connection for power to each of said image elements in each of said group;

a testing element, connectable to a plurality of said image elements, and operable when connected to said image elements to test each of said image elements in the group and report a result of said test.

15. An assembly as in claim 14, wherein said plurality of power lines and testing elements are on the same wafer.

16. An assembly as in claim 14, wherein said plurality

of power lines and said testing elements are on a physically separate wafer from said wafer that includes said image elements, and said physically separate wafer is connectable to said wafer.

17. An assembly as in claim 14, wherein said testing element tests each of the analog to digital converters in each of the image elements.

18. An assembly as in claim 17, wherein said testing elements causes said analog to digital converters to output each of the its plurality of output codes.

19. An assembly as in claim 17, wherein said testing element causes an input to a plurality of said analog to digital converters which changes in a first direction, and tests for a corresponding change in an output of said plurality of analog to digital converters.

20. An assembly as in claim 19, wherein said the changes comprise changing an integration time of light input to said image elements.

21. An assembly, comprising:

a wafer, including a plurality of separable image elements arranged in a linear direction;

a first power line, also arranged linearly, and arranged adjacent to a first group of said image elements, said first group collectively forming a linearly shaped group adjacent to said first power line;

a second power line, arranged linearly but spaced from said first power line, and arranged adjacent to a second group of said image elements, said second group collectively forming a linearly shaped group adjacent to said first power line but spaced from said first group;

a test structure, connected to one of said groups, and operable to test each of the image elements in said one of said groups during a time period When said one of said groups is receiving power.

22. An assembly as in claim 21, further comprising a third power line, also arranged linearly but spaced from said first power line and arranged adjacent to a third group of said image elements, said third group collectively forming a linearly shaped group adjacent to said first group, but spaced from said first group.

23. An assembly as in claim 21, wherein said first and second power lines and said test structure are on said wafer.

24. An assembly as in claim 21, wherein said first and second power lines and said test structure are on a separate wafer that is connectable to said wafer.